Amendments to the Drawings:

Figures 1-5 have been amended as required by including the designation "PRIOR ART" on the drawing. Corrected drawings in compliance with 37 CFR 1.121(d) have been attached.

REMARKS

The Applicant respectfully requests further examination and reconsideration in view of the amendments above and the arguments set forth fully below. Claims 1-23 were previously pending in this application. Within the Office Action, Claims 1-23 have been rejected. Accordingly, Claims 1-23 are currently pending.

Drawings

Within the Office Action, it is stated that Figures 1-5 should be designated by a legend such as –Prior Art –. By the above amendments, Figures 1-5 have been amended to include the designation "Prior Art" as suggested by the Examiner.

Rejections under 35 U.S.C. § 102

Within the Office Action, Claims 1-5, 7-17 and 19-22 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,243,538 to Okuzawa (hereinafter "Okuzawa"). The Applicant respectfully disagrees.

Okuzawa teaches a comparison and verification system for logic circuits and method thereof. Okuzawa teaches that when a hierarchy design is attempted in a logic design of a logic circuit, a system for verifying an equivalence between an upper level logic and a lower level logic is required. [Okuzawa, Abstract] When the two different level logics are compared, the logics are once converted to Boolean expressions regardless of logic expressions of the logics, involving a logic circuit diagram and a truth table, and Shannon's formula is applied to the two Boolean expressions under a same order of variables to be extracted, to thereby produce binary decision diagrams (BDDs). [Okuzawa, Abstract] When the equivalence between the produced BDDs is determined, the BDDs are simplified, respectively, and the simplified BDDs are integrated from the branches, and a determination can be carried out one time, without a repeat process. [Okuzawa, Abstract] Okuzawa does not teach programming a processing path according to a first substitute circuit which is not definable by a sequence of basic Boolean circuits. Okuzawa is directed to a comparison and verification system. Further, Okuzawa teaches producing the binary decision diagrams for the logic levels and then comparing them to determine whether the binary decision diagrams are equivalent. [Okuzawa, col. 2, lines 14-36] Okuzawa does not teach determining a first substitute circuit which is not definable by a sequence of basic Boolean circuits.

In contrast to the teachings of Okuzawa, the reduced architecture processing paths of the present invention reduce the throughput time of a processing path by substituting a reduced-transistor non-Boolean equivalent circuit in place of a sequence of traditional Boolean logic sequences. This reduction in throughput time increases the speed at which a microprocessor can process data. By reducing the number of transistors in a processing path, the present invention further reduces the power consumed by an integrated circuit and the resulting size of the chip. The reduced-transistor circuit is defined by the same truth table as the sequence of standard Boolean logic circuits, but is not definable by a sequence of standard Boolean logic circuits. A processing path of the integrated circuit is programmed with the reduced-transistor circuit instead of the sequence of standard Boolean circuits, thereby reducing the time delay of the processing path and the power consumed by the circuit. As described above, Okuzawa is directed to a comparison and verification system and does not teach programming a processing path according to a first substitute circuit which is not definable by a sequence of basic Boolean circuits.

The independent Claim 1 is directed to a method of designing an integrated circuit. The method of Claim 1 comprises programming a processing path within the integrated circuit according to a first substitute circuit comprising substitute inputs and a substitute output, wherein a truth table representing the first substitute circuit is identical to a truth table representing a first sequence of Boolean elements representing a processing path, and wherein the first substitute circuit is not definable by a sequence of basic Boolean circuits. As described above, Okuzawa is directed to a comparison and verification system and does not teach programming a processing path according to a first substitute circuit which is not definable by a sequence of basic Boolean circuits. For at least these reasons, the independent Claim 1 is allowable over the teachings of Okuzawa.

Claims 2-5 and 7-15 depend on the independent Claim 1. As described above, the independent Claim 1 is allowable over the teachings of Okuzawa. Accordingly, Claims 2-5 and 7-15 are all also allowable as being dependent on an allowable base claim.

The independent Claim 16 is directed to an apparatus for reducing a throughput time of a processing path of basic logic elements within an integrated circuit. The apparatus of Claim 16 comprises a programming module for programming a first substitute circuit into the processing path of the integrated circuit, wherein the substitute circuit is not defined by a sequence of basic Boolean circuits, and wherein the substitute circuit is defined by a truth table identical to a truth table defining a processing path comprised of basic Boolean circuits. As described above, Okuzawa is directed to a comparison and verification system and does not teach a programming

module for programming a processing path according to a first substitute circuit which is not definable by a sequence of basic Boolean circuits. For at least these reasons, the independent Claim 16 is allowable over the teachings of Okuzawa.

Claims 17 and 19-22 depend on the independent Claim 16. As described above, the independent Claim 16 is allowable over the teachings of Okuzawa. Accordingly, Claims 17 and 19-22 are all also allowable as being dependent on an allowable base claim.

Rejections under 35 U.S.C. § 103

Within the Office Action, Claims 6, 18 and 23 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Okuzawa in view of Applicant's Admitted Prior Art. The Applicant respectfully disagrees. As discussed above, Okuzawa does not teach programming a processing path according to a first substitute circuit which is not definable by a sequence of basic Boolean circuits. Okuzawa is directed to a comparison and verification system. Further, Okuzawa teaches producing the binary decision diagrams for the logic levels and then comparing them to determine whether the binary decision diagrams are equivalent. [Okuzawa, col. 2, lines 14-36] Okuzawa does not teach determining a first substitute circuit which is not definable by a sequence of basic Boolean circuits. As further recognized within the Office Action, Okuzawa does not explicitly disclose the integrated circuit is a MOS circuit. The background of the present application is cited for this proposition. However, the cited portion of the background section teaches

> [t]he process of designing and configuring an integrated circuit according to pre-determined transistor configurations is well known to those skilled in the art. Figures 1-4 illustrate *common Boolean gates* and the transistor equivalents currently used to represent these gates in a CMOS circuit. [Present Specification, page 2, lines 2-5, emphasis added]

It is not taught nor made obvious from the background section of the present application, reducing architecture processing paths and reducing the throughput time of a processing path by substituting a *reduced-transistor non-Boolean equivalent circuit* in place of a sequence of traditional Boolean logic sequences. Further, as described above, Okuzawa is directed to a comparison and verification system and does not teach programming a processing path according to a first substitute circuit which is not definable by a sequence of basic Boolean circuits. Accordingly, neither Okuzawa, the background section of the present application, nor their

combination teach programming a processing path according to a first substitute circuit which is not definable by a sequence of basic Boolean circuits.

Claim 6 is dependent on the independent Claim 1. Claim 18 is dependent on the independent Claim 16. As described above, the independent Claims 1 and 16 are both allowable over the teachings of Okuzawa. Accordingly, Claims 6 and 18 are both also allowable as being dependent on an allowable base claim.

The independent Claim 23 is directed to a method of programming a processing path comprising an input flip flop in a MOS integrated circuit. The method of Claim 23 comprises receiving a first sequence of basic Boolean elements, reducing the first sequence of basic Boolean elements to an equivalent sequence of elements, generating a substitute circuit from the equivalent sequence of elements and programming a processing path in the MOS integrated circuit according to the substitute circuit, wherein the substitute circuit is not definable by a sequence of basic Boolean elements, and wherein the substitute circuit is generated to define a truth table that also defines the first sequence of Boolean elements. As described above, neither Okuzawa, the background section of the present application, nor their combination teach programming a processing path according to a first substitute circuit which is not definable by a sequence of basic Boolean circuits. For at least these reasons, the independent Claim 23 is allowable over the teachings of Okuzawa, the background section of the present application and their combination.

For the reasons given above, Applicant respectfully submits that claims 1-23 are now in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, she is encouraged to call the undersigned attorney at (408) 530-9700.

Respectfully submitted,
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Date: April 11, 2006

By: _____
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CERTIFICATE OF MAILING (37 CFR§ 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

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Date: 4/11/06 By: _____